


<b>Form PTO-1449</b>  <b>U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE</b>  <b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>  (Use several sheets if necessary)	<b>Atty. Docket No.</b> 98095DIV4	<b>Serial No.:</b> 10/008,653  <div style="text-align: right; transform: rotate(-45deg);"> <b>RECEIVED</b>  <b>JUN 25 2002</b>  <b>NYC 2800 MAIL ROOM</b> </div>
	<b>Applicant</b> Gonzales	
	<b>Filing Date</b> November 9, 2001	<b>Group</b> 2815

## U. S. PATENT DOCUMENTS

Examiner Initial	Document Number	Issue Date	Patentee	Class	Sub-Class	Filing Date
h-v	4,470,852	Sep. 11, 1984	Ellsworth			

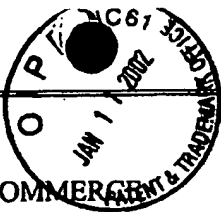
## FOREIGN PATENT OR PUBLISHED FOREIGN PATENT APPLICATION

Examiner Initial	Document Number	Public. Date	Country or Patent Office	Class	Sub-Class	Transl Y N

## OTHER DOCUMENTS

(Including Author, Title, Date, Relevant Pages, Place of Publication)

h-v	Wolf et al. (Silicon Processing For The VLSI ERA, Volume 1: Process Technology, pp. 397-399, 1986)
<b>Examiner</b> <i>[Signature]</i>	<b>Date Considered</b> 7/25/02
<b>EXAMINER:</b> Initial citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	



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U.S. DEPARTMENT OF COMMERCE  
PATENT AND TRADEMARK OFFICEINFORMATION DISCLOSURE  
STATEMENT BY APPLICANT

(Use several sheets if necessary)

Atty. Docket No.  
98095DIV3Serial No.  
10/008,653Applicant  
Gonzalez et al.Filing Date  
11/9/01

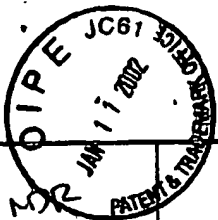
Group 2815

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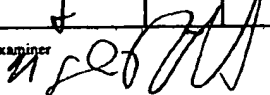
## FOREIGN PATENT OR PUBLISHED FOREIGN PATENT APPLICATION

Examiner Initial	Document Number	Public. Date	Country or Patent Office	Class	Sub-Class	Transl Y N



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		Wong, S. et al., "Elevated Source/Drain MOSFET," 1984 IEDM, December 9-12, 1984, pp. 634-37.
		Moravvej-Farshi, M. et al., "Novel Self-Aligned Polysilicon-Gate MOSFETS with Polysilicon Source and Drain," Solid-State Electronics, Vol. 30, No. 10, 1987, pp. 1053-62.
		Lynch, W. et al., "UPMOS-A New Approach to Submicron VLSI," Solid State Devices, 1988.
		Yamada, T. et al., "Spread/Source Drain (SSD) MOSFET Using Selective Silicon Growth for 64mbit DRAMs," 1989 IEDM, December 3-6, 1989, pp. 35-38.
		Shin, H. et al., "MOSFET Drain Engineering Analysis for Deep Submicron Dimensions: Part II - A New Structural Approach for Deep Submicron MOSFETs," SRC, November 1991.
		M. Togo et al., "A Gate-side Air-gap Structure (GAS) to Reduce the Parasitic Capacitance in MOSFET," 1996 Symposium on VLSI Technology Digest of Technical Papers, pp. 38-39.
		Makino, T. et al., "A Stacked Source Drain MOSFET Using Selective Epitaxy," Fujitsu Limited, Publication Date Unknown.
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